REMARKS

Claims 1-3 are rejected under 35 U.S.C. 102 (b) as being anticipated by Nshizawa et al. U.S. Patent No. 5,910,010A (hereinafter Nshizawa).

Claim 1 is amended to call for "A method of separately molding a plurality of semiconductor assemblies on separate multiple semiconductor substrates/leadframes." Claim 1 further calls for the steps of "providing vertically stacked molding die layers stacked one above the other to form vertically stacked die mold sections between said die layers for completely molding separate multiple semiconductor assemblies on separate substrates/leadframes in mold forming pockets in said die layers, said die layers having at least one top layer aperture or die hall in the top most die layer to from an opening into a top die mold section and a plurality of intermediate layer apertures or die halls in intermediate die layers to form openings into lower vertically stacked die mold sections, said top die mold section having runner grooves in at least one of said top die layer or next lower die layer with a separate runner groove extending directly from each of said top layer aperture to a separate one of said mold forming pockets in the top die mold section and said lower die sections having runner grooves in at least one of said die layers with a separate runner groove extending directly from each of said intermediate layer apertures to a separate one of said mold framing pockets in the die mold section for passing molding compound through the top layer aperture along said runner grooves to the mold framing pockets in the top die section and down through the plurality of intermediate layer apertures between the die mold layers along each said runner grooves into the mold forming pockets in the die mold layers in the lower die sections ." This is not shown or suggested by Nshizawa. Nshizawa teaches

to capsulate multiple chip on leadframe into one molded unit. Applicant's teaches separately molding a plurality of semiconductor assemblies on separate multiple semiconductor substrates/leadframes. This is not taught by Nshizawa. Applicant teaches providing vertically stacked molding die layers stacked one above the other for completely molding separate multiple semiconductor assemblies on separate substrates/leadframes in vertically stacked die mold sections between the die mold layers in mold forming pockets in said die mold layers. This is not taught by Nshizawa. Applicant further teaches the die mold layers have at least one top layer aperture or die hall in the top most die layer and a plurality of intermediate layer apertures or die halls in intermediate die layers and applicant further teaches the e top die mold section having runner grooves in at least one of the top die layer or next lower die layer with a separate runner groove extending directly from each of the top layer aperture to a separate one of the mold forming pockets in the top die mold section and further the lower die sections having runner grooves in at least one of the die layers with a separate runner groove extending directly from each of the intermediate layer apertures to a separate one of the mold forming pockets in the die mold section for passing molding compound through the top layer aperture along said runner grooves to the mold framing pockets in the top die section and down through the plurality of intermediate layer apertures between the die mold layers along each of the runner grooves into the mold forming pockets in the die mold layers in the lower die sections. This is not shown or suggested by Nshizawa. Claim 1 further calls for providing separate semiconductor substrates with semiconductor assemblies between each of said vertically stacked layers in the location of the mold forming pockets; and flowing molding compound through

the top layer into the substrate/ leadframe in the top die section and from the top die section through die halls between stacked die layers along the runners into the mold framing pockets to the other substrate/leadframes between stacked layers. This is not taught or suggest by Nshizawa. Claim 1 is therefore deemed allowable over the Nshizawa reference.

The present application is a continuing application of serial no. 10/225,425 filed August 22, 2002 in which there was a restriction requirement and the claims 1-3 were withdrawn. The application serial no. 10/225,425 has been allowed. The claims have been amended to also overcome the reference of Plummer U.S. Patent No. 4,480,975 that was cited in this prior application.

In view of the above applicants Claim 1 is deemed allowable.

Claim 2 is cancelled. Claim 3 dependent on Claim 1 is deemed allowable for at least the same reasons as Claim 1.

Applicant respectfully requests an early notice of allowance of Claims 1 and 3.

Respectfully submitted,

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